ABSTRACT OF THE DISCLOSURE

A low-pass filter configured as a switched capacitor circuit in which capacitor charge switching is performed by 2-phase clock signals that control respective sets of switching elements, wherein an interval between a first-phase clock signal pulse and a succeeding second-phase clock signal pulse, during which no charging/discharging of capacitors should occur, is made as short as possible while ensuring that the two sets of switching elements cannot enter the ON state simultaneously. A low cut-off frequency can thereby be achieved, while using very small capacitor values.